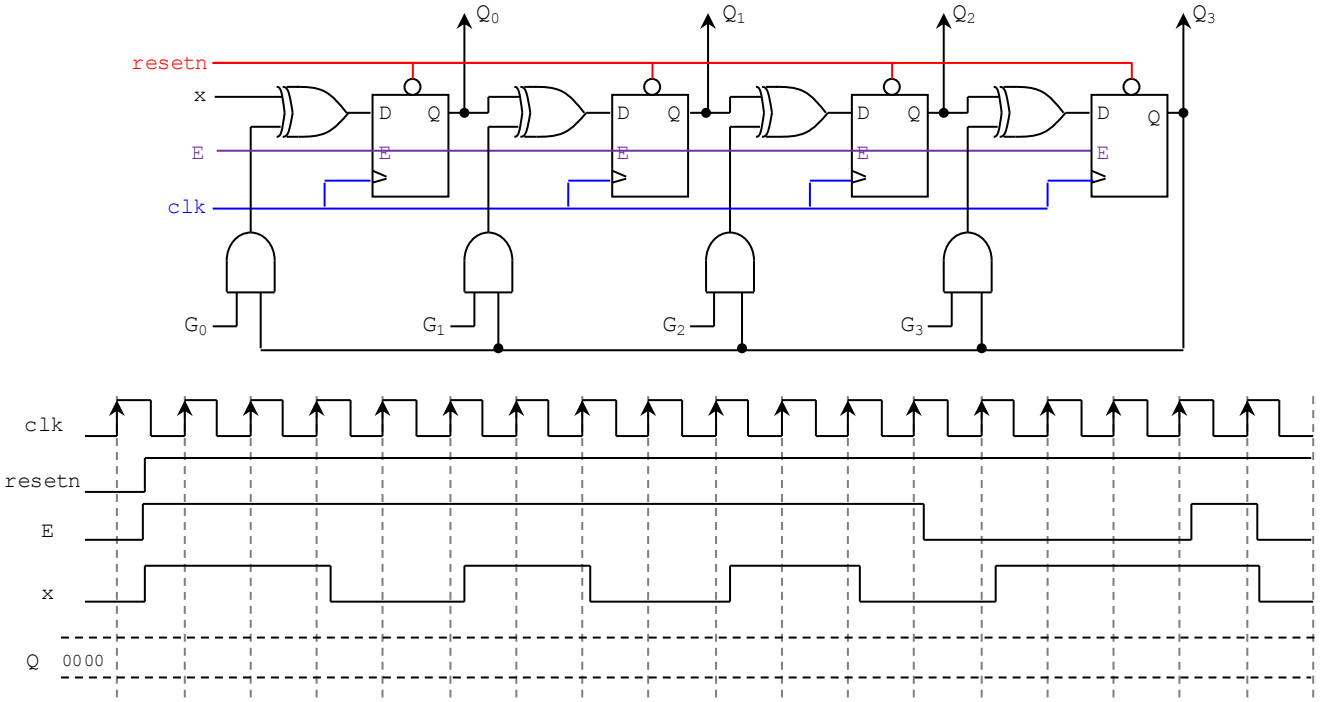
Final Exam

(December 11th @ 7:00 pm)

Presentation and clarity are very important! Show your procedure!

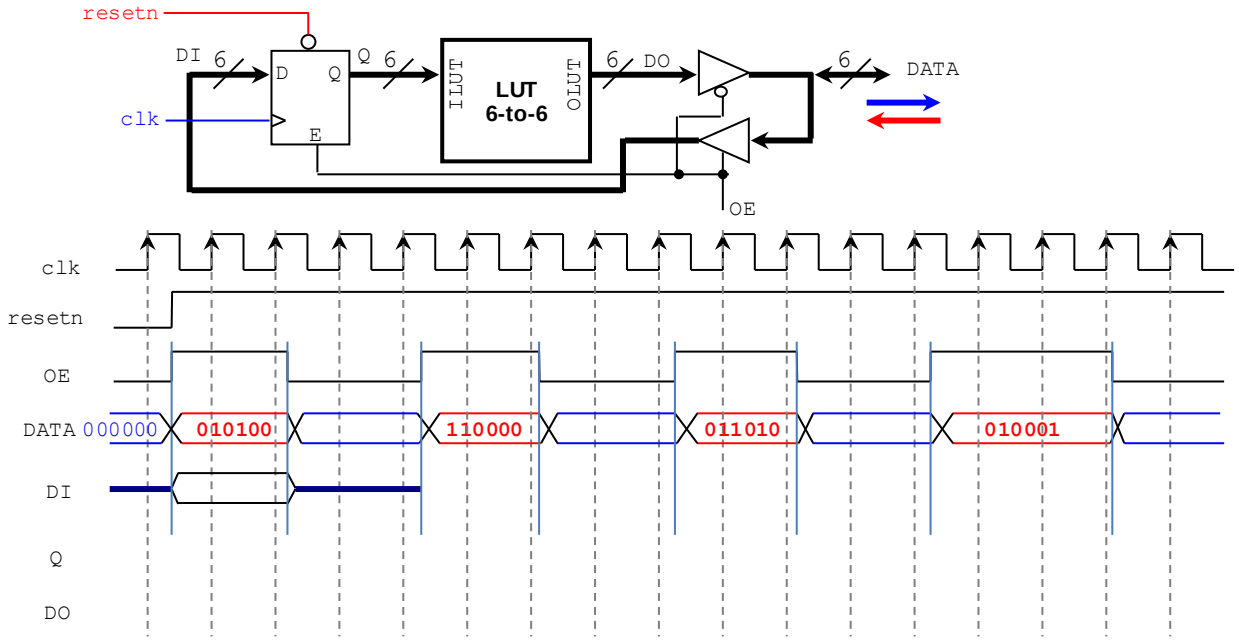
Problem 1 (12 pts)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 0110$, $Q = Q_3Q_2Q_1Q_0$



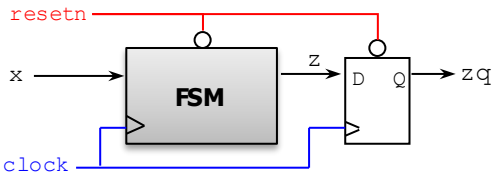
Problem 2 (11 pts)

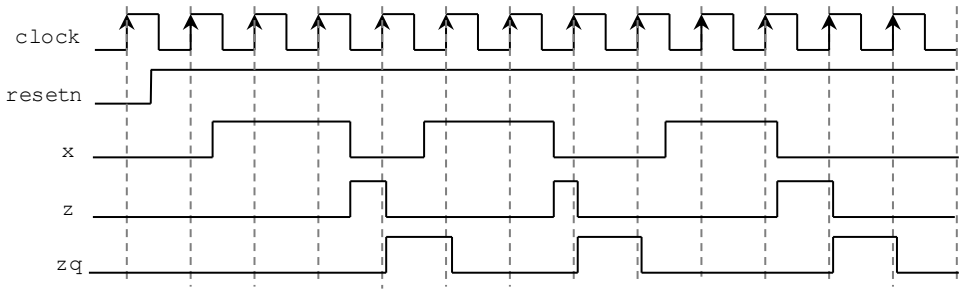
- Given the following circuit, complete the timing diagram.
  The LUT 6-to-6 implements the following function: $OLUT = \lceil sqrt(ILUT) \rceil$, where $ILUT$ is a 6-bit unsigned number.
  For example $ILUT = 41\ (101001_2) \rightarrow OLUT = \lceil sqrt(41) \rceil = 7\ (000111_2)$



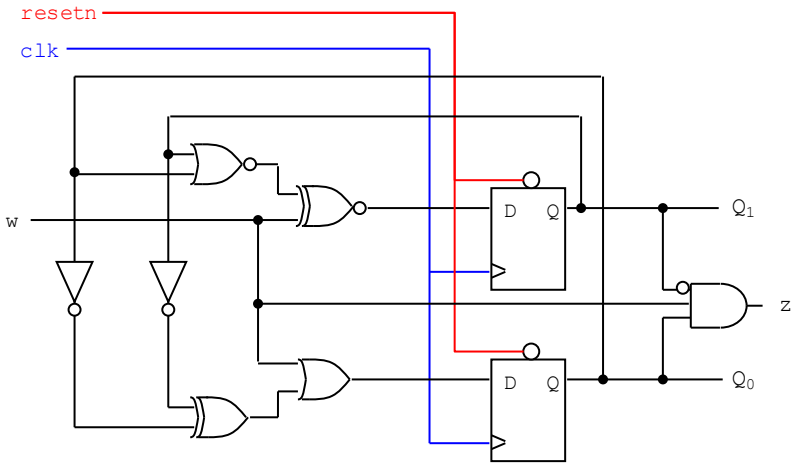
PROBLEM 3 (20 PTS)

- Pulse Detector: The circuit consists of a FSM and a flip flop. The timing diagram shows the behavior of the circuit. The flip flop makes sure that the output zq lasts for one clock cycle.
  Draw the State Diagram (any representation) of the given FSM (8 pts).



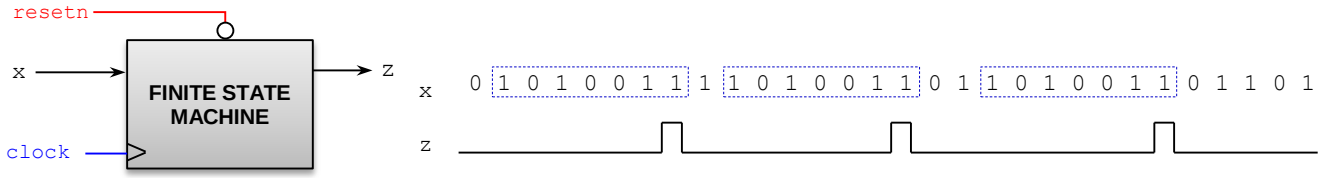


- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following Finite State Machine. Is it a Mealy or Moore FSM? (12 pts)



PROBLEM 4 (23 PTS)

- Sequence detector: The machine has to generate $z = 1$ when it detects the sequence 1010011. Once the sequence is detected, the circuit looks for a new sequence.



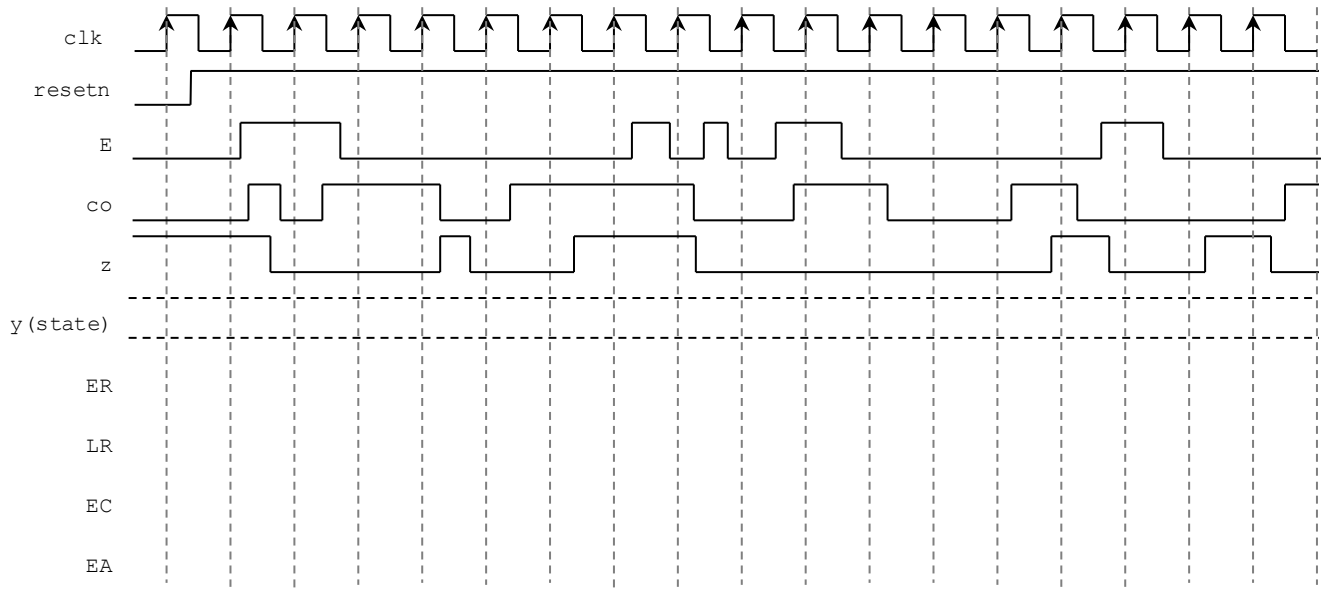
- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit with input x and output z. Is this a Mealy or a Moore machine? Why? (15 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (3 pts)

PROBLEM 5 (16 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity myfsm is
   port ( clk, resetn: in std_logic;
          z, E, co: in std_logic;
          ER,LR,EC,EA: out std_logic);
end myfsm;
```

```
architecture behavioral of myfsm is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, z, E, co)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if E = '1' then
               y <= S2;
            else
               y <= S1;
            end if;

          when S2 =>
            if z = '1' then y <= S3; else y <= S2; end if;

          when S3 =>
            if E = '1' then y <= S3; else y <= S1; end if;

        end case;
     end if;
  end process;

  Outputs: process (y, z, E, co)
  begin
      ER <= '0'; LR <= '0'; EC <= '0'; EA <= '0';
      case y is
         when S1 => ER <= '1'; EC <= '1';
                    if E = '1' then
                          EA <= '1';
                    end if;

         when S2 => ER <= '1'; EA <= '1';
                    if co = '1' then LR <= '1'; end if;
                    if z = '0' then EC <= '1'; end if;

         when S3 =>
      end case;
  end process;
end behavioral;
```



PROBLEM 6 (18 PTS)

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.